

1. A method to form a floating gate for a flash memory device, said method comprising:

forming a gate dielectric layer overlying a substrate;

depositing a conductor layer overlying said gate

5 dielectric layer;

depositing a masking layer overlying said ~~first~~
conductor layer;

forming conductive spacers on the sidewalls of said
conductor layer and said masking layer wherein said spacers
10 extend vertically above the top surface of said conductor
layer; and

etching away said masking layer to complete said
floating gate.

2. The method according to Claim 1 further comprising the
steps of:

forming a first dielectric layer overlying said
substrate; and

5 thereafter removing said first dielectric layer where
said first conductor layer of said floating gate is planned
prior to said step of forming a gate dielectric layer.

3. The method according to Claim 1 wherein said first dielectric layer is formed by thermal oxidation of said substrate.
4. The method according to Claim 3 wherein said gate dielectric layer is formed by thermal oxidation of said substrate.
5. The method according to Claim 1 wherein said first and second conductor layers comprise polysilicon.
6. The method according to Claim 1 further comprising the steps of:
 - forming a second dielectric layer overlying said floating gate and said substrate;
 - 5 forming a third conductor layer overlying said second dielectric layer; and
 - patterning said third conductor layer to form a control gate overlying said floating gate.
7. The method according to Claim 6 wherein part of said control gate overlies said substrate but not said floating gate.

8. The method according to Claim 7 further comprising implanting ions into said substrate to form doped regions adjacent to said control gate and to said floating gate.

9. A method to form a flash memory device, said method comprising:

forming a gate dielectric layer overlying a substrate;

depositing a first conductor layer overlying said gate

5 dielectric layer;

depositing a masking layer overlying said first conductor layer;

etching through said masking layer and said first conductor layer;

10 thereafter depositing a second conductor layer

overlying said masking layer, said first conductor layer, and said substrate;

etching down said second conductor layer to form spacers on said sidewalls of said first conductor layer and 15 said masking layer wherein said spacers extend vertically above the top surface of said first conductor layer;

etching away said masking layer to complete said floating gate;

20 forming a second dielectric layer overlying said floating gate and said substrate;

forming a third conductor layer overlying said second dielectric layer; and

patterning said third conductor layer to form a control gate overlying said floating gate.

10. The method according to Claim 9 further comprising the steps of:

forming a first dielectric layer overlying said substrate; and

5 thereafter removing said first dielectric layer where said first conductor layer of said floating gate is planned prior to said step of forming a gate dielectric layer.

11. The method according to Claim 9 wherein said first dielectric layer is formed by thermal oxidation of said substrate.

12. The method according to Claim 11 wherein said gate dielectric layer is formed by thermal oxidation of said substrate.

13. The method according to Claim 9 wherein said first and second conductor layers comprise polysilicon.

14. The method according to Claim 9 wherein part of said control gate overlies said substrate but not said floating gate.

15. The method according to Claim 14 further comprising implanting ions into said substrate to form doped regions adjacent to said control gate and to said floating gate.

16. A flash memory device comprising:

a substrate;

a floating gate overlying said substrate wherein said floating gate comprises:

5 a conductor layer overlying a dielectric layer;

and

conductive spacers adjacent to and contacting said first conductor layer wherein said spacers extend vertically above said conductor layer; and

10 a control gate overlying said floating gate with a second dielectric therebetween.

17. The device according to Claim 16 wherein said gate dielectric layer underlying said floating gate comprises a first thickness underlying said first conductor layer and a second thickness underlying said spacers.

18. The device according to Claim 16 wherein said first and second conductor layers comprise polysilicon.
19. The device according to Claim 16 wherein part of said control gate overlies said substrate but not said floating gate.
20. The device according to Claim 19 further comprising doped regions adjacent to said control gate and to said floating gate.